Patent Claims

1. A circuit arrangement

- having a terminal (1) for a high-frequency signal,

- having at least two additional signal leads (21a, 21b, 21c, 22a, 22b) which form transmission/reception paths,

- having a switching unit (3) for connecting the terminal (1) to a signal lead (21a, 21b, 21c, 22a, 22b),

- having a primary protection device (41) against electrostatic discharges which is connected between the terminal (1) and the switching unit (3),

- wherein the primary protection device (41) contains a first protective element (51) which diverts all voltage pulses whose pulse height exceeds 200 V to reference potential (7),

- wherein the first protective element (51) has a capacitance (8) which is less than 1 pF,

- wherein the first protective element (51) has an insertion loss which is less than 0.3 dB,

- wherein the switching unit (3) and the primary protection device (41) are integrated in or on a multilayer substrate.

2. The circuit arrangement as recited in claim 1,

wherein the first protective element (51) is a gallium arsenide double diode.

3. The circuit arrangement as recited in claim 1 or 2,

wherein the primary protection device (41) contains a lead (6), which connects the terminal (1) to the switching unit (3) and wherein the first protective element (51) connects the lead (6) to the reference potential (7).

4. The circuit arrangement as recited in one of claims 1 through 3,

wherein a second protective element (52) is connected in parallel to the first protective element (51).

5. The circuit arrangement as recited in claim 4,

wherein a capacitor (8) is connected in series to the lead (6) between the first protective element (51) and the second protective element (52).

6. The circuit arrangement as recited in one of claims 4 or 5,

wherein the second protective element (52) is a spark gap.

7. The circuit arrangement as recited in one of claims 4 or 5,

wherein the second protective element (52) is a polymer suppressor.

8. The circuit arrangement as recited in one of claims 4 or 5,

wherein the second protective element (52) is an overvoltage component whose capacitance is smaller than 1 pF.

9. The circuit arrangement as recited in one of claims 4 or 5,

wherein the second protective element (52) is an inductance greater than 18 nH.

10. The circuit arrangement as recited in one of claims 1 through 9,

- wherein one or a plurality of control leads (91, 92, 93) are provided for the control of the switching unit,

- wherein each control lead (91, 92, 93) is connected to a secondary protection device (42) against electrostatic discharges.

11. The circuit arrangement as recited in one of claims 1 through 10,

wherein a supply lead (100) for an operating voltage (VCC) is provided, the supply lead being connected to a secondary protection device (42) against electrostatic discharges.

12. The circuit arrangement as recited in one of claims 1 through 11,

- wherein the switching unit (3) contains two field effect transistors (111, 112), the break distance (121, 122) of each field effect transistor (111, 112) connecting the terminal (1) to a signal lead (21a, 21b, 21c, 22a, 22b).

- wherein each gate (131, 132) of each field effect transistor (111, 112) is connected to a control lead (91, 92),

- and wherein each gate (131, 132, 93) is connected to a secondary protection device (42) against electrostatic discharges.

13. The circuit arrangement as recited in one of claims 10 through 12, wherein a secondary protection device (42) contains a protective element (53a, 53b, 53c, 54) having a switching voltage that is lower than 100 V.

14. The circuit arrangement as recited in one of claims 10 through 13, wherein a secondary protection device (42) contains a protective element (53a, 53b, 53c, 54) which is a varistor.

15. The circuit arrangement as recited in one of claims 10 through 13, wherein a secondary protection device (42) contains a protective element (53a, 53b, 53c, 54) which is a Zener diode.

16. The circuit arrangement as recited in one of claims 10 through 15, wherein the one or a plurality of secondary protection devices (42) is connected to the reference potential (7).

17. The circuit arrangement as recited in one of claims 1 through 16,

wherein the switching unit (3) contains PIN diodes.

18. The circuit arrangement as recited in one of claims 1 through 16, wherein the switching unit (3) contains a gallium arsenide switch.

19. The circuit arrangement as recited in one of claims 1 through 18, wherein the terminal (1) is the antenna input of a mobile telephone.

20. The circuit arrangement as recited in one of claims 1 through 19, wherein the signal leads (21a, 21b, 21c, 22a, 22b) form transmission/reception paths of a mobile telephone.

21. The circuit arrangement as recited in one of claims 1 through 20, wherein the switching unit (3) and the primary protection device (41) are integrated in a multilayer ceramic substrate.